APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,512	10/14/2004	Jeroen Anton Johan Leijten	NL02 0321 US	4657

65913   7590   12/21/2010
NXP, B.V.
NXP INTELLECTUAL PROPERTY & LICENSING
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER
GIROUX, GEORGE

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
12/21/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>11 October 2010</u>.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-17</u> is/are pending in the application.

  4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-17</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

  a)☐ All b)☐ Some * c)☐ None of:

    1.☐ Certified copies of the priority documents have been received.

    2.☐ Certified copies of the priority documents have been received in Application No. _____.

    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

  * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

1.   This Office Action is in response to applicant's communication filed 11

October 2010, in response to the Office Action mailed 9 July 2010. The

applicant's remarks and any amendments to the claims or specification have

been considered, with the results that follow.

Specification

2.   The specification has not been checked to the extent necessary to

determine the presence of all possible minor errors. Applicant's cooperation is

requested in correcting any errors of which applicant may become aware in the

specification.

Claim Rejections - 35 USC § 112

3.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

4.   Claims 15 and 17 are rejected under 35 U.S.C. 112, second paragraph, as

being indefinite for failing to particularly point out and distinctly claim the subject

matter which applicant regards as the invention.

5.   Claim 15 recites the limitation "the register of the one of the second set of

one or more issue slots" in lines 3-4 and 7-8 and "the one of the second set of

one or more issue slots" in line 6. There is insufficient antecedent basis for either

of these limitations in the claim (both "*the* register" and "*the* one of the second set

of one or more issue slots".

6.   Claim 17 recites the limitation "the at least one other input path" in line 3.

There is insufficient antecedent basis for this limitation in the claim because it is

not clear to which input path (i.e., the second input path recited in claim 17 or the

input path of claim 13) this recitation refers. For the purposes of examination the

examiner assumes that the "other" input path is the first input path of claim 13.

7.   Claim 17 further recites the limitation "the instruction register" in lines 2-3.

There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

8.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for

all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described
> as set forth in section 102 of this title, if the differences between the subject matter sought to
> be patented and the prior art are such that the subject matter as a whole would have been
> obvious at the time the invention was made to a person having ordinary skill in the art to which
> said subject matter pertains. Patentability shall not be negatived by the manner in which the
> invention was made.

9.   Claims 1, 3, 4, 8 and 10 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Dally (US 6,192,384) in view of Garde (US 6,510,510).

        As per claim 1, Dally teaches a multi-issue processor comprising a

register file as **[a parallel processing computer system (column 1, lines 9-13)**

including a stream register file 14 (figure 1)]; and a plurality of issue slots as

[ALU clusters 0-7 (numeral 18, figure 1)], each one of the plurality of issue

slots including a plurality of functional units as **[each ALU cluster 18 includes a**

number of ALUs 26 (figures 2-3)], an input routing network that provides multiple data path outputs for a single data path input as **[crosspoint switch 30 distributes the inputs to the ALUs 26, from a single input from the stream register file (SRF) (figures 2-3)]**, the input routing network receiving data from the register file on the single data path input via a single data input path and providing data from the register file to functional units of the plurality of functional units, the data provided on the multiple data path outputs via multiple data output paths as **[crosspoint switch 30 outputs the operands to the ALUs 26, from a single input from the stream register file (SRF) 14 (figures 1-3 and column 4, lines 38-58)]**, and a plurality of holdable registers that hold duplicate data from the register file, wherein in a first set of the plurality of issue slots the holdable registers store data on the multiple data output paths of the first set as **[local register files 28 buffer the inputs to the ALUs 26 and store local constants, parameters and variables for the cluster, where the local register files 28 are fed by the crosspoint switch 30 (figures 1-3 and column 4, lines 38-58)]** and the holdable register do not store data on the single input path corresponding to the input routing networks of the first set **[local register files 28 buffer the inputs to the ALUs 26, directly at the inputs, and store local constants, parameters and variables for the cluster, where the local register files 28 are fed by the crosspoint switch 30 (figures 1-3 and column 4, lines 38-58)]**.

Dally does not explicitly teach a second set of the plurality of issue slots the holdable registers store data on the single data input path corresponding to

the input routing networks of the second set and the holdable registers do not

store data on the multiple data output paths of the second set. However, it has

been held that rearranging the parts of an invention (i.e. moving the holdable

registers from the output path to the input path of the routing network) involves

only routine skill in the art. *In re Japikse*, 86 USPQ 70. This is further evidenced

by the teachings of Garde, provided below.

Garde teaches a second set of the plurality of issue slots the holdable

registers store data on the single data input path corresponding to the input

routing networks of the second set as **[operand latch 132 holds the output of

the registers 130 on the input to the op busses 110 and 112, and

multiplexers 162 and 168 supply inputs from bus 110, bus 112 or bus 114 to

computation circuit 150 as operands A & B in response to a select A & B

signals (column 6, lines 3-47 and figure 2)]** and the holdable registers do not

store data on the multiple data output paths of the second set as **[operand latch

132 holds the output of the registers 130 on the input to the op busses 110

and 112, and multiplexers 162 and 168 supply inputs from bus 110, bus 112

or bus 114 to computation circuit 150 as operands A & B in response to a

select A & B signals (column 6, lines 3-47 and figure 2), where the

crosspoint switch 30 taught by Dally (see Dally, figure 3) serves as the

input routing network. Therefore, the holdable registers of the combined

issue slot(s) are on the single input path of the input routing network and

not on the final output paths of the input routing network]**.

Dally and Garde are analogous art, as they are within the same field of
endeavor, namely connecting a register file to multiple functional/computation
units.

It would have been obvious to one of ordinary skill in the art, at the time
the invention was made, to use the operand latches for the register file output of
Garde on the outputs of the stream register file/input to the crosspoint switches
for some of the clusters taught by Dally.

Because both Dally and Garde teach systems with a register file output
connected to a series of inputs of a number of functional/computational units, and
both including latches/registers on the path between the register file output and
the functional unit inputs, it would have been obvious to one of ordinary skill in
the art to use the operand latches for the register file output of Garde on the
outputs of the stream register file/input to the crosspoint switches for some of the
clusters taught by Dally, to achieve the predictable result of latching the output of
the stream register file before it is sent via the crosspoint switches to the various
ALUs. This also has the added advantage of decreasing the size/complexity of
the hardware, if the number of holdable registers is decreased.

As per claim 3, Dally teaches wherein the input routing network of each of
the plurality of issue slots has a plurality of data path inputs as **[the stream
register file sends data to the ALU clusters via the crosspoint switches
(figures 1-3) and crosspoint switch 30 outputs the operands to the ALUs
26, from a single input from the stream register file (SRF) 14 as well as an**

input from outputs of the other ALUs in the cluster (figures 1-3 and column 4, lines 38-58)].

Dally does not explicitly teach that in the second set of issue slots holdable registers of the plurality of holdable registers are located between each of the inputs of the input routing network and the register file. However, it has been held that rearranging the parts of an invention (i.e. moving the holdable registers from the output path to the input path of the routing network) involves only routine skill in the art. *In re Japikse*, 86 USPQ 70. This is further evidenced by the teachings of Garde, provided below.

Garde teaches the second set of issue slots' holdable registers of the plurality of holdable registers are located between each of the inputs of the input routing network and the register file as **[operand latch 132 holds the output of the registers 130 on the input to the op busses 110 and 112, and multiplexers 162 and 168 supply inputs from bus 110, bus 112 or bus 114 to computation circuit 150 as operands A & B in response to a select A & B signals (column 6, lines 3-47 and figure 2)]**.

Dally and Garde are analogous art, as they are within the same field of endeavor, namely connecting a register file to multiple functional/computation units.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use the operand latches for the register file output of Garde on the outputs of the stream register file/input to the crosspoint switches for some of the clusters taught by Dally.

Because both Dally and Garde teach systems with a register file output connected to a series of inputs of a number of functional/computational units, and both including latches/registers on the path between the register file output and the functional unit inputs, it would have been obvious to one of ordinary skill in the art to use the operand latches for the register file output of Garde on the outputs of the stream register file/input to the crosspoint switches for some of the clusters taught by Dally, to achieve the predictable result of latching the output of the stream register file before it is sent via the crosspoint switches to the various ALUs. This also has the added advantage of decreasing the size/complexity of the hardware, if the number of holdable registers is decreased.

As per claim 4, Dally teaches wherein, in the first set of issue slots, holdable registers are located between the input routing networks and each of the plurality of function units as **[local register files 28 buffer the inputs to the ALUs 26 and store local constants, parameters and variables for the cluster, where the local register files 28 are fed by the crosspoint switch 30 (figures 1-3 and column 4, lines 38-58)]**.

As per claim 8, see the rejection of claim 1, above.

As per claim 10, see the rejection of claim 4, above.

10.   Claims 2, 5-7, 9, 11 and 12 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Dally (US 6,192,384) in view of Garde (US 6,510,510), and

further in view of Fisher (US 6,026,479).

As per claim 2, Dally teaches the multi-issue processor of claim 1, as

described above.

Dally does not teach a first instruction set accessing at least the first set of

issue slots; and a second instruction set accessing the second set of issue slots,

however.

Fisher teaches "a first instruction set accessing at least the first set of

issue slots; and a second instruction set accessing the second set of issue slots"

as **["A CPU having a cluster VLIW architecture...which operates in both a

high instruction level parallelism (ILP) mode and a low ILP mode. In high

ILP mode, the CPU executes wide instruction words using all operational

clusters of the CPU and all of a main instruction cache and main data

cache of the CPU are accessible to a high ILP task. The CPU also includes

a mini-instruction cache, a mini-instruction register and a mini-data cache

which are inactive during high ILP mode. An instruction level controller in

the CPU receives a low ILP signal, such as an interrupt or function call to a

low ILP routine, and switches to low ILP mode. In low ILP mode, the main

instruction cache and main data cache are deactivated to preserve their

contents. At the same time, a predetermined cluster remains active while

the remaining clusters are also deactivated. The low ILP task executes

instructions from the mini-instruction cache which are input to the**

predetermined cluster through the mini-instruction register. The mini-data cache stores operands for the low ILP task"(abstract, lines 1-19)].

Dally and Fisher are analogous art, as they are within the same field of endeavor, namely instruction processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the parallel processor with a register file connected to a number of ALU clusters via crosspoint switches controlling the inputs of the functional units of each ALU in the clusters, taught by Dally, with the multiple instruction sets and multiple groupings of resources for each, as taught Fisher, while using the latch locations taught by Garde for the separate resource cluster taught by Fisher.

The motivation for doing so is provided by Fisher as **["the separate mini-instruction cache and mini-data cache along with the use of only the predetermined cluster minimizes the pollution of the main instruction and data caches, as well as pollution of register files in the deactivated clusters, with regard to a task executing in high ILP mode"(abstract, lines 20-24)]**.

As per claim 5, Dally teaches the multi-issue processor of claim 1, as described above.

Dally does not teach wherein the first set of issue slots are accessed by a first set of instructions for a VLIW processor and the second set of issue slots are

accessed by a second set of instructions that are used by an interrupt routine, however.

Fisher teaches wherein the first set of issue slots are accessed by a first set of instructions for a VLIW processor and the second set of issue slots are accessed by a second set of instructions that are used by an interrupt routine as

["A CPU having a cluster VLIW architecture…which operates in both a high instruction level parallelism (ILP) mode and a low ILP mode. In high ILP mode, the CPU executes wide instruction words using all operational clusters of the CPU and all of a main instruction cache and main data cache of the CPU are accessible to a high ILP task. The CPU also includes a mini-instruction cache, a mini-instruction register and a mini-data cache which are inactive during high ILP mode. An instruction level controller in the CPU receives a low ILP signal, such as an interrupt or function call to a low ILP routine, and switches to low ILP mode. In low ILP mode, the main instruction cache and main data cache are deactivated to preserve their contents. At the same time, a predetermined cluster remains active while the remaining clusters are also deactivated. The low ILP task executes instructions from the mini-instruction cache which are input to the predetermined cluster through the mini-instruction register. The mini-data cache stores operands for the low ILP task" (abstract, lines 1-19)].

Dally and Fisher are analogous art, as they are within the same field of endeavor, namely instruction processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the parallel processor with a register file connected to a number of ALU clusters via crosspoint switches controlling the inputs of the functional units of each ALU in the clusters, taught by Dally, with the multiple instruction sets and multiple groupings of resources for each, as taught Fisher, while using the latch locations taught by Garde for the separate resource cluster taught by Fisher.

The motivation for doing so is provided by Fisher as **["the separate mini-instruction cache and mini-data cache along with the use of only the predetermined cluster minimizes the pollution of the main instruction and data caches, as well as pollution of register files in the deactivated clusters, with regard to a task executing in high ILP mode"(abstract, lines 20-24)]**.

As per claim 6, Fisher teaches wherein the second set of instructions has fewer instructions than the first set of instructions as **[An embodiment of a method for reducing cache pollution in a CPU, according to the present invention, includes providing a main instruction cache configured to store VLIW instructions, wherein each VLIW instruction is further comprised of a plurality of c-instructions, providing a plurality of operational clusters, wherein each one of the plurality of operational clusters is configured to receive one of the plurality of c-instructions of each VLIW instruction in the main instruction cache, and executing a high ILP task by loading VLIW**

**instructions from the main instruction cache into a main instruction
register for output to the plurality of clusters. The method includes
receiving a low ILP signal and, responsive thereto, deactivating the main
instruction cache and main instruction register, deactivating the plurality of
operational clusters, except for a predetermined one of the operational
clusters, activating a mini-instruction cache and a mini-instruction register,
and serially executing a low ILP task by serially loading c-instructions from
the mini-instruction cache into the mini-instruction cache for output to the
predetermined one of the operational clusters (column 4, lines 16-34)].**

As per claim 7, Dally teaches the multi-issue processor of claim 1, as
described above.

Dally does not explicitly teach wherein the first set of issue slots has more
issue slots than the second set of issue slots, however.

Fisher teaches wherein the first set of issue slots has more issue slots
than the second set of issue slots as **["The CPU also includes a mini-
instruction cache, a mini-instruction register and a mini-data cache which
are inactive during high ILP mode. An instruction level controller in the
CPU receives a low ILP signal, such as an interrupt or function call to a low
ILP routine, and switches to low ILP mode. In low ILP mode, the main
instruction cache and main data cache are deactivated to preserve their
contents. At the same time, a predetermined cluster remains active while
the remaining clusters are also deactivated. The low ILP task executes**

instructions from the mini-instruction cache which are input to the
predetermined cluster through the mini-instruction register. The mini-data
cache stores operands for the low ILP task"(abstract, lines 6-19) wherein
deactivating some clusters means the cluster running the low ILP tasks
(the second set of issue slots) is smaller than the first].

Dally and Fisher are analogous art, as they are within the same field of
endeavor, namely instruction processing.

At the time of the invention it would have been obvious to a person of
ordinary skill in the art to combine the parallel processor with a register file
connected to a number of ALU clusters via crosspoint switches controlling the
inputs of the functional units of each ALU in the clusters, taught by Dally, with the
multiple instruction sets and multiple groupings of resources for each, as taught
Fisher, while using the latch locations taught by Garde for the separate resource
cluster taught by Fisher.

The motivation for doing so is provided by Fisher as ["the separate mini-
instruction cache and mini-data cache along with the use of only the
predetermined cluster minimizes the pollution of the main instruction and
data caches, as well as pollution of register files in the deactivated
clusters, with regard to a task executing in high ILP mode"(abstract, lines
20-24)].

As per claim 9, see the rejection of claim 2, above.

As per claim 11, see the rejection of claim 6, above.

As per claim 12, see the rejection of claim 7, above.

11.   Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dally (US 6,192,384) in view of Garde (US 6,510,510), further in view of Fisher (US 6,026,479), and further in view of Martonosi (US 6,745,336).

As per claim 13, see the rejection of claim 2, above, except that while Dally/Garde/Fisher teaches the issue slots and associated holdable registers, including those located on each respective input of the functional units, it does not explicitly teach the issue slot configured to reduce power usage by preventing switching of combinatorial gates in each respective one of the plurality of functional units, in the issue slot, during clock cycles when the functional unit is not in use.

Martonosi teaches a first issue slot configured to reduce power usage by preventing switching of combinatorial gates in each respective one of the plurality of functional units, in the issue slot, during clock cycles when the functional unit is not in use **[latches 30 and 34 latch operand inputs for the functional unit 40 (figure 1), while bit detect units provide condition signals to prevent switching of latches when the operand(s) of the latches are not in use to reduce power consumption (column 4, line 39 to column 5, line 22; column 5, line 53 to column 6, line 27; etc.)]**.

Dally/Garde/Fisher and Martonosi are analogous art, as they are within
the same field of endeavor, namely instruction processing utilizing latches
between the register file and functional units to latch operands.

It would have been obvious to one of ordinary skill in the art, at the time
the invention was made, to use the detection logic/signals and gating of
Martonosi used to prevent swtiching of unused latches, in the holdable
registers/latches taught by Dally/Garde/Fisher.

The motivation for doing so would have been to reduce power
consumption of the system (see Martonosi, column 4, line 39 to column 5, line
22; column 5, line 53 to column 6, line 27; etc.).

As per claim 14, see the rejection of claim 2, above.

As per claim 15, Dally/Garde/Fisher/Martonosi teaches wherein in
response to the interrupt signal, the multi-issue processor is further configured to
retrieve a data value from a register of the one of the second set of one or more
issue slots **[upon receiving a low-ILP interrupt signal, the processor
deactivates the main caches and activates the mini-instruction and mini-
data caches and executes the low-ILP instructions using the new resources
(Fisher: abstract, etc.), where the instruction level controller 140 also
performs a register store of the registers within register file 152D for later
restoration at the completion of the low ILP task (Fisher: column 6, lines 8-
25)]**, execute the interrupt service routine using only one or more of the

functional units of the one of the second set of one or more issue slots **[upon receiving a low-ILP interrupt signal, the processor deactivates the main caches and activates the mini-instruction and mini-data caches and executes the low-ILP instructions using the new resources (Fisher: abstract, etc.)]**, and restore the register of the one of the second set of one or more issue slots to the retrieved data value **[the instruction level controller 140 also performs a register store of the registers within register file 152D for later restoration at the completion of the low ILP task (Fisher: column 6, lines 8-25)]**.

As per claim 16, see the rejection of claim 13, above.

As per claim 17, Dally/Garde/Fisher/Martonosi teaches wherein for each of the second set of issue slots the input routing network includes at least a second input path coupled to the instruction register **[the mini-instruction register 132 is connected to the instruction controller/functional units (Fisher: figure 2, etc.)]**, the at least one other input path each including a register coupled to store data on the at least second input path **[see the holdable registers taught by Dally/Garde/Fisher, above]**.

Response to Arguments

12.　　Applicant's arguments filed 11 October 2010 have been fully considered but they are not persuasive.

13.　　Applicant argues that the proposed combination would "undermine either the operation or the purpose of the main reference", arguing that in the proposed combination the crosspoint switch would only be able to transfer a single item to each ALU.

　　　　However, Garde teaches that multiple operands may be latched at the input of the routing network and provided to the computation unit (or units) (see, e.g., Garde: figure 2). Furthermore, the Dally reference does not require that a single item be moved over the routing network at a time, as suggested by applicant. Rather, Dally teaches that multiple values may distributed simultaneously (see, e.g., Dally: column 4, lines 47-5 and column 6, line 60 to column 7, line 8).

14.　　In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

15.   Applicant also argues that the cited art does not teach a second set of
issue slots that have holdable registers on the single data input path of the input
routing network and do not have holdable registers on the multiple data output
paths of the input routing network.

        However, Garde teaches operand latch 132 holds the output of the
registers 130 on the input to the op busses 110 and 112, and multiplexers 162
and 168 supply inputs from bus 110, bus 112 or bus 114 to computation circuit
150 as operands A & B in response to a select A & B signals (column 6, lines 3-
47 and figure 2). The multiplexers, used for switching, are a part of the input
routing network taught by Garde, and there are no holdable registers on the
output paths of the multiplexers, or on the inputs of the computation circuits. In
the combination of Dally and Garde, provided above, the crosspoint switch 30
taught by Dally (see Dally, figure 3) serves as the input routing network.
Therefore, the holdable registers of the combined issue slot(s) are on the single
input path of the input routing network and not on the final output paths of the
input routing network.

16.   In response to applicant's argument that the examiner's conclusion of
obviousness is based upon improper hindsight reasoning, it must be recognized
that any judgment on obviousness is in a sense necessarily a reconstruction
based upon hindsight reasoning. But so long as it takes into account only
knowledge which was within the level of ordinary skill at the time the claimed
invention was made, and does not include knowledge gleaned only from the

applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*,
443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Furthermore, the test for
obviousness is not whether the features of a secondary reference may be bodily
incorporated into the structure of the primary reference; nor is it that the claimed
invention must be expressly suggested in any one or all of the references.
Rather, the test is what the combined teachings of the references would have
suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208
USPQ 871 (CCPA 1981).

Conclusion

17.   The following is a summary of the treatment and status of all claims in the
application as recommended by **M.P.E.P. 707.07(i)**: claims 1-17 are rejected.

18.   The prior art made of record and not relied upon is considered pertinent to
applicant's disclosure.

    a.   Balmer (US 2002/0108026) -- discloses holdable registers on
    register file outputs for transferring data between datapaths.

    b.   Hao (4,594,655) -- discloses staging registers on the outputs of the
    register file for holding operands to be sent to the ALUs.

19.   Applicant's amendment necessitated the new ground(s) of rejection
presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**.

See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as
set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire
THREE MONTHS from the mailing date of this action. In the event a first reply is
filed within TWO MONTHS of the mailing date of this final action and the advisory
action is not mailed until after the end of the THREE-MONTH shortened statutory
period, then the shortened statutory period will expire on the date the advisory
action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be
calculated from the mailing date of the advisory action. In no event, however, will
the statutory period for reply expire later than SIX MONTHS from the date of this
final action.

20.   The examiner requests, in response to this Office action, that support be
shown for language added to any original claims on amendment and any new
claims. That is, indicate support for newly added claim language by specifically
pointing to page(s) and line number(s) in the specification and/or drawing
figure(s). This will assist the examiner in prosecuting the application.

21.   When responding to this office action, Applicant is advised to clearly point
out the patentable novelty which he or she thinks the claims present, in view of
the state of the art disclosed by the references cited or the objections made. He
or she must also show how the amendments avoid such references or
objections. See 37 CFR 1.111(c).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GEORGE D. GIROUX whose telephone number is (571)272-9769. The examiner can normally be reached on Monday through Friday, 9:30am - 6:00pm E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/   /George D Giroux/
Supervisory Patent Examiner, Art Unit 2183   Examiner, Art Unit 2183